AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (PREVIOUSLY PRESENTED) A circuit comprising:

a first pad circuit configured to transfer a first data signal in response to a pad control signal;

a second pad circuit configured to generate a second data signal from an input signal in response to said pad control signal;

a core logic configured to (i) exchange said first data signal with said first pad circuit, (ii) receive said second data signal and (iii) generate a control signal;

a first cell configured to (i) transfer said first data signal between said first pad circuit and said core logic and (ii) swap said first data signal and a test signal;

a second cell configured to (i) transfer said second data signal from said second pad circuit to said core logic and (ii) swap said second data signal and said test signal; and

a test circuit configured to (i) exchange said test data signal with said first cell and said second cell, (ii) store a test control signal and (iii) multiplex said test control signal and said control signal to generate said pad control signal.

2. (PREVIOUSLY PRESENTED) The circuit according to claim 1, wherein (i) said test circuit transfers said test data signal to said first cell and (ii) said first cell overwrites said first data signal with said test data signal for transfer to said first pad circuit.

3. (PREVIOUSLY PRESENTED) The circuit according to claim 2, wherein said test circuit is further configured to clock said test data signal at a predetermined time to cause said first pad circuit to undergo a predetermined state transition for a transition response measurement of said first pad circuit.

4. (PREVIOUSLY PRESENTED) The circuit according to claim 1, wherein (i) said second cell transfers said second data signal to said second cell and (ii) said second cell overwrites said test data signal with said second data signal for transfer to said test circuit.

5. (PREVIOUSLY PRESENTED) The circuit according to claim 4, wherein said test circuit is further configured to clock said test data signal to receive a sequence of samples for said second data signal as said input signal undergoes a predetermined state transition for a transition response measurement of said second pad circuit.

6. (PREVIOUSLY PRESENTED) The circuit according to claim 1, wherein said test circuit comprises:

a multiplexer configured to multiplex said control signal and said test control signal to generate said pad control signal; and

a controller configured to (i) store said test control signal, (ii) transfer said test control signal to said multiplexer, and (iii) exchange said test data signal with said first cell and said second cell.

7. (ORIGINAL) The circuit according to claim 6, wherein said controller comprises:

an input configured to receive said test control signal; and

a user data register configured to (i) store said test control signal from said input and (ii) present said test control signal to said multiplexer.

8. (CANCELED)

9. (CURRENTLY AMENDED) A method of testing a pad circuit that transfers a data signal in response to a pad control signal, the method comprising the steps of:

(A) generating a test control signal ~~generated~~ by a test circuit;

(B) multiplexing said test control signal and a control signal generated by a core logic co-located with said test circuit to generate said pad control signal;

(C) configuring said pad circuit with information from said test control signal;

(D) swapping said data signal of said pad circuit and a test data signal of a cell after step (C); and

(E) measuring a response of said pad circuit based upon said test data signal.

10. (PREVIOUSLY PRESENTED) The method according to claim 9, wherein step (D) comprises the sub-steps of:

transferring said test data signal to said cell;

first overwriting said data signal with said test data signal; and

first transferring said data signal to said pad circuit in response to said first overwriting.

11. (PREVIOUSLY PRESENTED) The method according to claim 10, wherein step (D) further comprises the sub-steps of:

clocking said test data signal after said first transferring of said data signal to said pad circuit;

second overwriting said data signal with said test data signal; and

second transferring said data signal to said pad circuit in response to said second overwriting, wherein said response of said pad circuit comprises a transition response for driving an output signal.

12. (CANCELED)

13. (PREVIOUSLY PRESENTED) The method according to claim 9, wherein step (D) comprises the sub-steps of:

first receiving said data signal at said cell;

first overwriting said test data signal with said data signal; and

first transferring said test data signal from said cell to said test circuit.

14. (PREVIOUSLY PRESENTED) The method according to claim 13, wherein step (D) further comprises the sub-steps of:

second receiving said data signal;

second overwriting said test data signal with said data signal; and

second transferring said test data signal from said cell to said test circuit, wherein said response of said pad circuit comprises a transition response to an input signal.

15. (CANCELED)

16. (CURRENTLY AMENDED) A circuit comprising:

means for generating a test control signal;

means for multiplexing said test control signal and a control signal generated by a core logic co-located with said means for generating;

means for transferring a data signal, said means for transferring being configured ~~by a first~~ with information from said test control signal;

~~means for generating a second control signal;~~

means for swapping said data signal of said means for transferring and a test data signal of a cell after configuring said means for transferring;

~~generating a third control signal;~~

~~means for multiplexing said third control signal and said second control signal to generate said first control signal;~~ and

means for measuring a response of said means for transferring based upon said test data signal.

17. (PREVIOUSLY PRESENTED) The circuit according to claim 1, wherein said pad control signal comprises an enable signal configured to alternatively enable and disable an output drive capability of said first pad circuit.

18. (PREVIOUSLY PRESENTED) The circuit according to claim 1, wherein said pad control signal comprises a receive enable signal configured to alternatively enable and disable a receive capability of said first pad circuit.

19. (PREVIOUSLY PRESENTED) The circuit according to claim 1, wherein said pad control signal comprises a signal configured to alternatively enable and disable an active termination of said second pad circuit.

20. (PREVIOUSLY PRESENTED) The circuit according to claim 1, wherein said pad control signal comprises a signal configured to control a noise margin threshold of said second pad circuit for said input signal.

21. (PREVIOUSLY PRESENTED) The circuit according to claim 1, wherein said control signal comprises a plurality of signals and said multiplexer comprises a plurality of multiplexers, one for each of said signals.

22. (PREVIOUSLY PRESENTED) The circuit according to claim 21, wherein at least one of said first pad circuit and said second pad circuit receives a subset of said signals.

23. (PREVIOUSLY PRESENTED) The circuit according to claim 16, wherein said response for said means for transferring is a transition response between a high state and a low state.